

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor layer;

5 a first insulating film formed on said semiconductor layer;

a first electrode layer formed on said first insulating layer;

10 an element isolating region comprising an element isolating insulating film formed to extend through said first electrode layer and said first insulating film to reach an inner region of said semiconductor layer, said element isolating region isolating an element region and being self-aligned with said first electrode layer;

15 a second insulating film formed on said first electrode layer and said element isolating region, an open portion exposing a surface of said first electrode layer being formed in said second insulating film; and

20 a second electrode layer formed on said second insulating film and said exposed surface of said first electrode layer, said second electrode layer being electrically connected to said first electrode layer via said open portion.

2. A semiconductor device comprising:

a semiconductor layer;

25 a first insulating film formed on said semiconductor layer;

a first electrode layer formed on said first

insulating layer;

an element isolating region comprising an element isolating insulating film formed to extend through said first electrode layer and said first insulating film to reach an inner region of the semiconductor layer, said element isolating region isolating an element region and being self-aligned with said first electrode layer;

a second insulating film formed on said first electrode layer and said element isolating region, an open portion exposing a surface of said first electrode layer being formed in said second insulating film;

a second electrode layer formed on said second insulating film; and

a third electrode layer formed on said second electrode layer and said exposed surface of said first electrode layer, said third electrode layer being electrically connected to said first electrode layer via said open portion.

3. The semiconductor device according to claim 1, wherein said first and second electrodes comprise a gate electrode of a selective transistor included in a NAND type flash memory.

4. The semiconductor device according to claim 2, wherein said first, second and third electrodes comprise a gate electrode of a selective transistor included in a NAND type flash memory.

5. The semiconductor device according to claim 1,

which is a semiconductor device in a memory cell array region, comprising:

said semiconductor layer;

5 said first insulating film formed on said semiconductor layer;

said first electrode layer formed on said first insulating layer;

10 said element isolating region comprising an element isolating insulating film formed to extend through said first electrode layer and said first insulating film to reach an inner region of said semiconductor layer, said element isolating region isolating an element region and being self-aligned with said first electrode layer;

15 said second insulating film formed on said first electrode layer and said element isolating region; and

said second electrode layer formed on said second insulating film;

20 wherein a surface of said element isolating region of said memory cell array region is arranged below a surface of said first electrode layer.

6. The semiconductor device according to claim 2, which is a semiconductor device in a memory cell array region, comprising:

25 said semiconductor layer;

said first insulating film formed on said semiconductor layer;

said first electrode layer formed on said first insulating layer;

said element isolating region comprising an element isolating insulating film formed to extend through said first electrode layer and said first insulating film to reach an inner region of said semiconductor layer, said element isolating region isolating an element region and being self-aligned with said first electrode layer;

said second insulating film formed on said first electrode layer and said element isolating region;

said second electrode layer formed on said second insulating film; and

said third electrode layer formed on said second electrode layer;

wherein a surface of said element isolating region of said memory cell array region is arranged below a surface of said first electrode layer.

7. The semiconductor device according to claim 5, wherein said first electrode layer performs a function of a floating gate and said second electrode layer performs a function of a control gate in said memory cell array region.

8. The semiconductor device according to claim 6, wherein said first electrode layer performs a function of a floating gate and said second and third electrode layers perform a function of a control gate in said

memory cell array region.

9. The semiconductor device according to claim 1,
wherein said first and second electrode layers comprise
a gate electrode in a peripheral circuit region formed
5 around a memory cell array region.

10. The semiconductor device according to claim 1,
wherein said first and second electrode layers comprise
a gate electrode in a peripheral circuit region formed
around a memory cell array region, and said second
10 insulating film of said peripheral circuit region being
removed completely.

11. The semiconductor device according to claim 1,
further comprising a connecting member arranged above
said element isolating region and electrically
15 connected to said second electrode layer.

12. The semiconductor device according to claim 2,
further comprising a connecting member arranged above
said element isolating region and electrically
connected to said third electrode layer.

13. The semiconductor device according to claim 1,
further comprising a connection member arranged above
said element region in which said second insulating
film is present and electrically connected to said
20 second electrode layer.

14. The semiconductor device according to claim 1,
further comprising a wiring electrically connected to
said second electrode layer via a connecting member,

wherein said wiring and said first electrode layer are connected to each other via said second electrode layer extending from said element region onto said element isolating region.

5 15. The semiconductor device according to claim 2, further comprising a wiring electrically connected to said third electrode layer via a connecting member, wherein said wiring and said first electrode layer are connected to each other via said third electrode layer
10 extending from said element region onto said element isolating region.

15 16. The semiconductor device according to claim 1, which is a semiconductor device in which said first and second electrode layers form a gate electrode, and a plurality of said gate electrodes are arranged on a chip, wherein widths of said open portions of said gate electrodes are equal to each other.

20 17. The semiconductor device according to claim 2, which is a semiconductor device in which said first, second and third electrode layers form a gate electrode, and a plurality of said gate electrodes are arranged on a chip, wherein widths of said open portions of said gate electrodes are equal to each other.

25 18. The semiconductor device according to claim 1, which is a semiconductor device in which said first and second electrode layers form a gate electrode, wherein

a plurality of said open portions are formed within said gate electrodes and the widths of said open portions are equal to each other.

19. The semiconductor device according to claim 2,
5 which is a semiconductor device in which said first, second and third electrode layers form a gate electrode, wherein a plurality of said open portions are formed within said gate electrodes and the widths of said open portions are equal to each other.

10 20. The semiconductor device according to claim 18, wherein said open portions are formed to cross each other.

21. The semiconductor device according to claim 19, wherein said open portions are formed to
15 cross each other.

22. The semiconductor device according to claim 18, wherein the distances between the adjacent open portions are equal to each other.

23. The semiconductor device according to
20 claim 19, wherein the distances between the adjacent open portions are equal to each other.

24. The semiconductor device according to claim 1,
which is a semiconductor device comprising a plurality of selective transistors formed said first and second
25 electrode layers in a NAND type flash memory, and a peripheral circuit transistor formed said first and second electrode layers,

said second insulating film of said plural selective transistors includes said open portion, and said second insulating film of said peripheral circuit transistor includes a plurality of said open portions, and a first distance between the adjacent open portions of said plural selective transistors is equal to a second distance between the adjacent open portions within a gate electrode of said peripheral circuit transistor.

25. The semiconductor device according to claim 2, which is a semiconductor device comprising a plurality of selective transistors formed said first, second and third electrode layers in a NAND type flash memory, and a peripheral circuit transistor formed said first, second and third electrode layers,

said second insulating film of said plural selective transistors includes said open portion, and said second insulating film of said peripheral circuit transistor includes a plurality of said open portions, and a first distance between the adjacent open portions of said plural selective transistors is equal to a second distance between the adjacent open portions within a gate electrode of said peripheral circuit transistor.

26. The semiconductor device according to claim 24, wherein said second distance is defined on a basis of said first distance.

27. The semiconductor device according to claim 25, wherein said second distance is defined on a basis of said first distance.

28. The semiconductor device according to claim 1,
5 which is a semiconductor device in which a gate electrode is formed of said first and second electrode layers, and said open portion is formed in said gate electrode, wherein said open portion extends from above said element region onto said element isolating region
10 in a direction of a channel width of said gate electrode.

29. The semiconductor device according to claim 2,
which is a semiconductor device in which a gate electrode is formed of said first, second and third
15 electrode layers, and said open portion is formed in said gate electrode, wherein said open portion extends from above said element region onto said element isolating region in a direction of a channel width of said gate electrode.

30. The semiconductor device according to claim 1,
20 wherein a thickness of said second electrode layer when deposited is at least half a width of said open portion.

31. The semiconductor device according to claim 2,
25 wherein a thickness of said third electrode layer when deposited is at least half a width of said open portion.

32. The semiconductor device according to claim 1,
wherein an electric resistance of said second electrode
layer is lower than that of said first electrode layer,
and said second electrode layer comprises of a metal
5 layer including a high melting point or a lamination
layer film comprising a metal silicide layer including
a high melting point and a polysilicon layer.

33. The semiconductor device according to claim 2,
wherein an electric resistance of said second and third
10 electrode layers is each lower than that of said first
electrode layer, and said second and third electrode
layers comprise of a metal layer including a high
melting point or a lamination layer film comprising a
metal silicide layer including a high melting point and
15 a polysilicon layer.

34. The semiconductor device according to claim 1,
wherein said second insulating film comprises of a
complex insulating film including a silicon nitride
film.

35. The semiconductor device according to claim 2,
wherein said second insulating film comprises of a
complex insulating film including a silicon nitride
film.

36. The semiconductor device according to claim 1,
25 which is a semiconductor device in which a gate
electrode is formed of said first and second electrode
layers, wherein said second insulating film remains at

an edge portion of said gate electrode.

37. The semiconductor device according to claim 2,
which is a semiconductor device in which a gate
electrode is formed of said first, second and third
5 electrode layers, wherein said second insulating film
remains at an edge portion of said gate electrode.

38. A semiconductor device, which is a NAND type
flash memory comprising a memory cell array region
provided a memory transistor including a first
10 electrode layer performing a function of a floating
gate and a second electrode layer performing a function
of a control gate, and a selective gate region provided
a selective transistor formed adjacent to said memory
cell array region, and a peripheral circuit region
15 arranged around said memory cell array region, said
NAND type flash memory comprising:

a semiconductor layer common with said memory cell
array region, said selective gate region and said
peripheral circuit region;

20 a first insulating film formed on said
semiconductor layer, said first insulating film being
formed commonly with said memory cell array region,
said selective gate region and said peripheral circuit
region;

25 a first electrode layer formed on said first
insulating film commonly with said memory cell array
region, said selective gate region and said peripheral

circuit region;

an element isolating region comprising an element
isolating insulating film extending through said first
electrode layer and said first insulating layer to
5 reach an inner region of said semiconductor layer, said
electrode isolating region being formed in each of said
memory cell array region, said selective gate region
and said peripheral circuit region, and said electrode
isolating region isolating an element region and being
10 self-aligned with said first electrode layer;

a second insulating film formed on said first
electrode layer and said element isolating region
commonly with said memory cell array region, said
selective gate region and said peripheral circuit
15 region, said second insulating film in said selective
gate region and said peripheral circuit region
including an open portion exposing a surface of said
first electrode layer; and

a second electrode layer formed on said second
20 insulating film and said exposed surface of said first
electrode layer, said second electrode layer being
formed commonly with said memory cell array region,
said selective gate region and said peripheral circuit
region and being electrically connected to said first
25 electrode layer via said open portion.

39. A semiconductor device, which is a NAND type
flash memory comprising a memory cell array region

provided a memory transistor including a first
electrode layer performing a function of a floating
gate and a second electrode layer performing a function
of a control gate, and a selective gate region provided
5 a selective transistor formed adjacent to said memory
cell array region, and a peripheral circuit region
arranged around said memory cell array region, said
NAND type flash memory comprising:

10 a semiconductor layer common with said memory cell
array region, said selective gate region and said
peripheral circuit region;

15 a first insulating film formed on said
semiconductor layer, said first insulating film being
formed commonly with said memory cell array region,
said selective gate region and said peripheral circuit
region;

20 a first electrode layer formed on said first
insulating film commonly with said memory cell array
region, said selective gate region and said peripheral
circuit region;

25 an element isolating region comprising an element
isolating insulating film extending through said first
electrode layer and said first insulating layer to
reach an inner region of said semiconductor layer, said
element isolating region being formed in each of said
memory cell array region, said selective gate region
and said peripheral circuit region, and said element

isolating region isolating an element region and being self-aligned with said first electrode layer;

a second insulating film formed on said first electrode layer and said element isolating region commonly with said memory cell array region, said selective gate region and said peripheral circuit region, said second insulating film in said selective gate region including a open portion exposing between a surface of said first electrode and partly a surface of said element isolating region formed adjacent to said first electrode layer; and

a second electrode layer formed on said second insulating film and said exposed surface of said first electrode layer commonly with said memory cell array region, said selective gate region and said peripheral circuit region, said second electrode layer being electrically connected to said first electrode layer via said open portion.

40. A method of manufacturing a semiconductor device in a selective gate region provided a selective gate transistor formed adjacent to a memory cell array region, comprising:

forming a first insulating film on a semiconductor layer;

forming a first electrode layer on said first insulating film;

forming an element isolating region comprising an

element isolating insulating film extending through
said first electrode layer and said first insulating
film to reach an inner region of said semiconductor
layer, said element isolating region isolating an
5 element region;

forming a second insulating film on said element
isolating region and said first electrode layer;

forming an open portion within said second
insulating film to expose a surface of the first
10 electrode layer;

forming a second electrode layer on said second
insulating film and said exposed surface of said first
electrode layer; and

selectively removing said first electrode layer,
15 said second insulating film and said second electrode
layer to form a gate electrode.

41. A method of manufacturing a semiconductor
device in a selective gate region provided a selective
gate transistor formed adjacent to a memory cell array
20 region, comprising:

forming a first insulating film on a semiconductor
layer;

forming a first electrode layer on said first
insulating film;

25 forming an element isolating region comprising an
element isolating insulating film extending through
said first electrode layer and said first insulating

film to reach an inner region of said semiconductor layer, said element isolating region isolating an element region;

forming a second insulating film on said element isolating region and said first electrode layer;

forming a second electrode layer on said second insulating film;

forming an open portion within said second insulating film to expose a surface of said first electrode layer;

forming a third electrode layer on said second electrode layer and said exposed surface of said first electrode layer; and

selectively removing said first electrode layer, said second insulating film, said second electrode layer and said third electrode layer to form a gate electrode.

42. A method of manufacturing a semiconductor device in a selective gate region provided a selective gate transistor formed adjacent to a memory cell array region, comprising:

forming a first insulating film on a semiconductor layer;

forming a first electrode layer on said first insulating film;

forming an element isolating region comprising an element isolating insulating film extending through

5 forming a second insulating film on said element
isolating region and said first electrode layer;
 forming a second electrode layer on said second
insulating film;
 forming a first mask layer on said second
10 electrode layer;
 forming a groove comprising a pair of mutually
facing side surfaces in said first mask layer, said
groove being formed to expose partly a surface of said
second electrode layer;
15 forming a side wall comprising a second mask layer
on said exposed side surface of said groove;
 selectively removing said second electrode layer
and said second insulating film by using said first and
second mask layers to form an open portion exposing a
20 surface of said first electrode layer;
 removing said first and second mask layers;
 forming a third electrode layer on said second
electrode layer and said exposed surface of said first
electrode layer; and
25 selectively removing said first electrode layer,
said second insulating film, said second electrode
layer and said third electrode layer to form a gate

electrode.

43. The method of manufacturing a semiconductor device according to claim 40, wherein said second insulating film remains at an edge portion of said gate electrode when formed said gate electrode.

44. The method of manufacturing a semiconductor device according to claim 41, wherein said second insulating film remains at an edge portion of said gate electrode when formed said gate electrode.

45. The method of manufacturing a semiconductor device according to claim 42, wherein said second insulating film remains at an edge portion of said gate electrode when formed said gate electrode.

46. The method of manufacturing a semiconductor device according to claim 40, further comprising removing an upper portion of said element isolating insulating film after formation of said element isolating region to position said removed upper portion of said element isolating insulating film below a surface of said first electrode layer.

47. The method of manufacturing a semiconductor device according to claim 41, further comprising removing an upper portion of said element isolating insulating film after formation of said element isolating region to position said removed upper portion of said element isolating insulating film below a surface of said first electrode layer.

48. The method of manufacturing a semiconductor device according to claim 42, further comprising removing an upper portion of said element isolating insulating film after formation of said element isolating region to position said removed upper portion of said element isolating insulating film below a surface of said first electrode layer.

49. The method of manufacturing a semiconductor device according to claim 40, further comprising forming a connecting member electrically connected to said second electrode layer, said connecting member being formed above said element isolating region.

50. The method of manufacturing a semiconductor device according to claim 41, further comprising forming a connecting member electrically connected to said third electrode layer, said connecting member being formed above said element isolating region.

51. The method of manufacturing a semiconductor device according to claim 42, further comprising forming a connecting member electrically connected to said third electrode layer, said connecting member being formed above said element isolating region.

52. The method of manufacturing a semiconductor device according to claim 40, further comprising forming a connecting member electrically connected to said second electrode layer, said connecting member being formed above said element region in which said

second insulating film is present.

53. The method of manufacturing a semiconductor device according to claim 41, further comprising forming a connecting member electrically connected to said third electrode layer, said connecting member being formed above said element region in which said second insulating film is present.

54. The method of manufacturing a semiconductor device according to claim 42, further comprising forming a connecting member electrically connected to said third electrode layer, said connecting member being formed above said element region in which said second insulating film is present.

55. The method of manufacturing a semiconductor device according to claim 40, wherein said second electrode layer is formed in a thickness that is at least half a width of said open portion.

56. The method of manufacturing a semiconductor device according to claim 41, wherein said third electrode layer is formed in a thickness that is at least half a width of said open portion.

57. The method of manufacturing a semiconductor device according to claim 42, wherein said third electrode layer is formed in a thickness that is at least half a width of said open portion.

58. The method of manufacturing a semiconductor device according to claim 40, wherein a surface of said

second electrode layer is planarized after formation of said second electrode layer.

5 59. The method of manufacturing a semiconductor device according to claim 41, wherein a surface of said third electrode layer is planarized after formation of said third electrode layer.

10 60. The method of manufacturing a semiconductor device according to claim 42, wherein a surface of said third electrode layer is planarized after formation of said third electrode layer.